

above Amendments and the following Remarks, Applicants respectfully request that the Examiner reconsider the outstanding objections and rejections and they be withdrawn.

Rejections Under 35 U.S.C. §102

In the Office Action, claims 18-21 have been rejected under 35 U.S.C. §102(e)(b) for being anticipated by U. S. Patent No. 5,259,881 issued to Edwards, *et al.* (“Edwards”). This rejection is respectfully traversed.

In this response, claim 19-21 have been cancelled, and claim 18 has been amended to clarify the difference between the claimed invention and the applied reference. Amended claim 18 recites “An apparatus for depositing a layer on a substrate, comprising: ... a deposition chamber depositing *a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer* by chemical vapor deposition; and a sputter chamber depositing *a metal layer* on the doped amorphous silicon layer by sputtering, wherein *the substrate is transferred from said deposition chamber to said sputter chamber in a vacuum*”.

Thus, according to the present invention, (a) the gate insulating layer, the amorphous silicon layer and the doped amorphous silicon layer are formed on the substrate in the deposition chamber, (b) the substrate is transferred to the sputter chamber in a vacuum, and (c) the metal layer is formed on the doped amorphous silicon of the substrate in the sputter chamber. Also, in the claimed apparatus, these are performed in sequence.

In Edwards, the cluster tool 10 shown in Fig. 1 includes a CVD module 30 and sputtering modules 24 and 28. However, Edwards fails to teach or suggest that the CVD module 30 is used to deposit a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon on the substrate having a gate wire pattern formed thereon. Also, Edwards fails to teach or suggest

that the sputter modules 24 and 28 are used to deposit a metal layer over the doped amorphous layer. Furthermore, Edwards is silent as to how the cluster tool 10 performs preheating, deposition and sputtering in the sequence described in claim 1.

For these reasons, it is submitted that claim 18 is patentable over Edwards. Applicants respectfully request that the rejection over claim 18 be withdrawn.

In the Office Action, claims 18-21 have been rejected under 35 U.S.C. §102(e)(b) for being anticipated by U. S. Patent No. 5,512,320 issued to Turner, *et al.* ("Turner"). This rejection is respectfully traversed.

As previously mentioned, in the claimed invention, (a) the gate insulating layer, the amorphous silicon layer and the doped amorphous silicon layer are formed on the substrate in the deposition chamber, (b) the substrate is transferred to the sputter chamber in a vacuum, and (c) the metal layer is formed on the doped amorphous silicon of the substrate in the sputter chamber. Also, in the claimed apparatus, these are performed in sequence.

In this regard, Turner fails to show an element that is corresponding to the claimed sputter chamber. Also, Turner shows the CVD chambers 40, 42, 44 and 46 but there is no teaching or suggestion that those CVD chambers 40, 42, 44 and 46 are used to deposit a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon on the substrate having a gate wire pattern formed thereon. Furthermore, Turner fails to teach or suggest that the vacuum system shown in Fig. 1 performs preheating, deposition and sputtering in the sequence described in claim 1.

For these reasons, it is submitted that claim 18 is patentable over Turner. Applicants respectfully request that the rejection over claim 18 be withdrawn.

Rejections Under 35 U.S.C. §103

In the Office Action, claims 18-21 have been rejected under 35 U.S.C. §103(a) for being unpatentable over Turner. This rejection is respectfully traversed.

As previously mentioned, Turner fails to teach or suggest an element corresponding to the claimed sputter chamber. Also, Turner fails to teach or suggest that the CVD chambers 40, 42, 44 and 46 are used to deposit a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon on the substrate having a gate wire pattern formed thereon. Furthermore, Turner fails to teach or suggest that the vacuum system shown in Fig. 1 performs preheating, deposition and sputtering in the sequence described in claim 1.

As well known, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art (MPEP 2143.03). Since Turner fails to teach or suggest (a) the sputter chamber, (b) the gate insulating layer, the amorphous silicon layer and the doped amorphous silicon from by the CVD chamber, and (c) the process sequence comprising preheating, deposition and sputtering, it is submitted that claim 18 is patentable over Turner. Accordingly, Applicants respectfully request that the rejection over claim 18 be withdrawn.

In the Office Action, claims 18-21 have been rejected under 35 U.S.C. §103(a) for being unpatentable over Edwards in view of Turner. This rejection is respectfully traversed.

As previously mentioned, Edward fails to teach or suggest that the CVD module 30 in Fig. 1 is used to deposit a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon on the substrate having a gate wire pattern formed thereon. Also, Edwards fails to teach or suggest that the sputter modules 24 and 28 are used to deposit a metal layer over

the doped amorphous layer. Furthermore, Edwards is silent as to how the cluster tool 10 performs preheating, deposition and sputtering in the sequence described in claim 1.

It is submitted that Turner fails to cure the deficiency from the teachings of Edwards. As mentioned above, Turner also fails to Since Turner fails to teach or suggest (a) the sputter chamber, (b) the gate insulating layer, the amorphous silicon layer and the doped amorphous silicon from by the CVD chamber, and (c) the process sequence comprising preheating, deposition and sputtering. Thus, it would not have been obvious to combine the teachings of Edwards and Turner to arrive at the claimed invention.

Accordingly, Applicants respectfully request that the rejection over claim 18 be withdrawn.

CONCLUSION

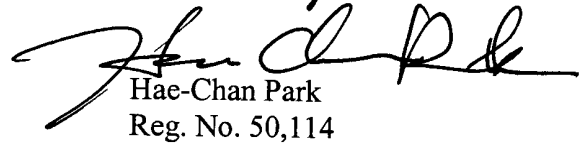
All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn.

Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claim 18 is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

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09/781,987

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,



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APPENDIX

The “marked-up” version of the amended specification is as follows.

18. (Amended) An apparatus for depositing a layer on a substrate, comprising:
- a load lock chamber [that receives] receiving a substrate having a gate wire pattern
formed thereon;
- a preheat chamber [that heats] receiving the substrate from said load lock chamber and
heating the substrate before deposition;
- a [chemical vapor] deposition chamber [that deposits thin layers] depositing a gate
insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by [a] chemical
vapor deposition [method]; and
- a sputter [process] chamber [that deposits] depositing a metal layer on [the substrate] the
doped amorphous silicon layer by [a] sputtering [method],
- wherein the substrate is transferred [among the chambers] from said deposition chamber
to said sputter chamber in a vacuum [while not exposed to an ambient atmosphere].

APPENDIX B

The “marked-up” version of the amended claims is as follows: